CLAIMS

What is claimed is:

1. A method for testing the electrical characteristics of a semiconductor integrated circuit, said method comprising the step of:

configuring an outer layer surrounding an inside needle, wherein said outer layer comprises a hard material which can penetrate through at least one semiconductor layer to thereby permit subsequent testing of at least one semiconductor integrated circuit component located below said semiconductor layer.

2. The method of claim 1 further comprising the step of:

permitting said inside needle to electrically contact said at least one semiconductor integrated circuit component located below said at least one semiconductor layer.

3. The method of claim 1 further comprising the step of:

configuring said inside needle to comprise a prober.

4. The method of claim 1 further comprising the step of :

configuring said outer layer to comprise a piercer.

5. The method of claim 1 further comprising the step of:

configuring said outer layer to comprise diamond.

6. The method of claim 1 further comprising the step of:

configuring said outer layer to comprise carborundum.

7. The method of claim 1 further comprising the step of:

configuring said inside needle to comprise a conductive metal prober.

8. The method of claim 1 further comprising the step of:

forming a concentric double layer structure prober formed from said inside needle and said outer layer.

9. The method of claim 1 further comprising the step of:

configuring said outer layer to comprise a sheath formed from a hard dielectric material, such that said sheath comprises a piercer.

10. A method for testing the electrical characteristics of a semiconductor integrated circuit, said method comprising the steps of:

a piercer comprising a hard material, wherein said piercer permits enhanced piercing of at least one semiconductor layer to thereby test at least one semiconductor integrated circuit component located below said at least one semiconductor layer; and

a dummy probe card for establishing an electrical contact path between a conductive electrical prober thereof and said at least one semiconductor layer, thereby permitting subsequent electrical measurement of said at least one semiconductor integrated circuit component.

11. The method of claim 10 wherein said hard material comprises diamond.

12. The method of claim 10 wherein said hard material comprises carborundum.

13. The method of claim 10 wherein said conductive electrical prober comprises a round tip metal probe which can pierce through a Cu process path prior to Cu electrical interconnections thereof.

14. An apparatus for testing the electrical characteristics of a semiconductor integrated circuit, said apparatus comprising:

an outer layer surrounding an inside needle; and

said outer layer comprising a hard material, which can penetrate through a semiconductor layer to permit subsequent testing of at least one semiconductor integrated circuit component located below said semiconductor layer.

15. The apparatus of claim 14 wherein said inside needle is adapted to electrically contact said at least one semiconductor integrated circuit component located below said semiconductor layer.

16. The apparatus of claim 14 wherein said inside needle comprises a prober.

17. The apparatus of claim 14 wherein said outer layer comprises a piercer.

18. The apparatus of claim 14 wherein said outer layer comprises diamond.

19. The apparatus of claim 14 wherein said outer layer comprises carborundum.

20. The apparatus of claim 14 wherein said inside needle comprises a conductive metal prober.

21. The apparatus of claim 14 wherein said inside needle and said outer layer together form a concentric double layer structure prober.

22. The apparatus of claim 14 wherein said outer layer comprises a sheath formed from a hard dielectric material, such that said sheath comprises a piercer.

23. An apparatus for testing the electrical characteristics of a semiconductor integrated circuit, said apparatus comprising:

a piercer comprising a hard material, wherein said piercer permits enhanced piercing of at least one semiconductor layer to thereby test at least one semiconductor integrated circuit component located below said at least one semiconductor layer; and

a dummy probe card for establishing an electrical contact path between a conductive electrical prober thereof and said at least one semiconductor layer, thereby permitting subsequent electrical measurement of said at least one semiconductor integrated circuit component.

24. The apparatus of claim 23 wherein said hard material comprises diamond.

25. The apparatus of claim 23 wherein said hard material comprises carborundum.

26. The apparatus of claim 23 wherein said conductive electrical prober comprises a round tip metal probe which can pierce through a Cu process path prior to Cu electrical interconnections thereof.